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Compute Project

PROPOSED STANDARDIZATION OF CHIPLET MODELS FOR HETEROGENEOUS INTEGRATION

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Introduction and Scope

This paper addresses the many questions surrounding the topic of model exchange for chiplet based designs. Specifically, this paper addresses the questions from the Chiplet Vendor's point view - what models need to be provided for chiplet; which models are mandatory and which are optional; what are the models used for; etc.

This paper is organized as follows: first, it provides an introduction to what is defined as a chiplet; then it lists all models with a brief description; this is followed by a detailed description of the model and how it might be used; then examples are provided of exchange of chiplet power and thermal models.

OCP Principles

Efficiency

This paper provides a comprehensive overview of chiplet models and is intended to inform chiplet vendors of models that should be provided with their chiplets

Scale

This paper sets a baseline for chiplet models, thus enabling integration planning of large chiplet systems.

Openness

This paper is licensed under the terms of Creative Commons license and is free for anyone to use.

Impact

We are hoping that this will further enable a scalable, open chiplet ecosystem and marketplace.

Definition and Characteristics of a Chiplet

A chiplet can be defined as a die specifically designed and optimized for operation within a package in conjunction with other chiplets. The interfaces used are the main differentiator. This differs from a conventional die which has the drive strength available to enable signaling over a longer electrical distance. A chiplet would not normally be able to be packaged separately and still operate effectively. The optimization of a chiplet to operate within a package can be summarized in the following key metrics on the chiplet-to-chiplet interface:

- Energy efficiency (pJ/bit)

- Bandwidth per beachfront (Gbps/mm)
- Area Efficiency (Gbps/mm²)
- Latency (ns)
- Reach (mm)
- Pitch (μm)

This list is not exhaustive as other metrics may also be applicable. A chiplet will generally have considerably lower energy consumption per bit given that it only needs to drive millimeters (or several 10's of millimeters) of distance. The latency of these connections is also optimized for most applications given the need to have these chiplets operate efficiently with one another.

These chiplet interfaces can be either characterized as highly parallel or serial. Serial interfaces that are optimized for chiplet operation, such as BoW, USR (ultra short reach) or XSR (extra short reach) interfaces tend to have wider interconnect pitches that can enable signaling on conventional packaging laminates. These are normally in the 130 μm pitch range but can be as low as 90 μm pitch

Chiplet interfaces that are considered highly parallel will have tighter pitches in the 30-80 μm pitch range. These pitches require enhancements to a package such as the integration of an interposer, a bridge or fanout technology to name a few options. Examples of these types of interfaces are OpenHBI, HBM, and BoW Fine.

Chiplets are also applicable in 3D operation.

WorkFlow Need for Chiplet Based Design

The workflow for a chiplet based design will be gated by the most constrained chiplet in the system. This constraint may come in the form of the finest pitch, heat dissipation, area, etc. If we take the example of a pitch limited system, such as one using an HBM memory stack, then the workflow would have to include that capability. Having a system that can handle a HBM also makes it capable of also utilizing a similarly defined interface such as OpenHBI.

Mixing of disparate chiplet interface types can be cost prohibitive. This is the case even with interfaces complying to the same base standard such as BoW and FoW fine were one interface may have a 130 μm pitch and the other may have a 40 μm pitch.

Selection of the interface standards to use in planning a schiplet must take into account the systems that are expected to use these chiplets and what capabilities those systems will have. Introducing a new chiplet that has a more difficult constraint will make this chiplet less attractive to integrate.

Chiplet Design Exchange (CDX) Charter

Domain Specific Acceleration is a key driver to improve the efficiency and economics of computational systems as Moore's law changes from covering a single chip to a system of chiplets and other components. Open Domain Specific Architecture (ODSA) is a sub-project under the Server Project of The Open Compute Project Foundation (OCP). OCP has a mission to apply the benefits of open source and open collaboration to hardware and rapidly increase the pace of innovation in, near and around the data center. ODSA follows the same mission in the area of multi-die and chiplet integration for domain specific architecture. The group is organized in several work streams to address a variety of architecture issues and standardization related to heterogeneous integrated circuits. These workstreams have produced notable die-to-die interface specifications such as for Bunch of Wire (BoW) and High Bandwidth Interconnect (Open HBI) that industry is benefiting from. Significantly more work is in progress all to the benefit of semiconductor industry revitalization and open collaboration.

Chiplet Design Exchange (CDX) Workstream of ODSA focuses on electrical, mechanical, and thermal design exchange standards related to chiplets and chiplet integration in the context of multi chiplet modules, 2.5D stacked, and 3D Integrated Circuits (3D-ICs). The big idea is to enable the foundation for the creation of a market for chiplets as modeled after the silicon IP business for single chip silicon and components business for electronics parts. The charter of the group is to identify needs and develop guidance and standards for design automation data models that the chip designers need to buy chiplets from third parties and be successful in high volume manufacturing of chiplet-based integrated circuits.

Development of such guidance and standards needs collaboration across architects, designers, design automation flows, electronic design automation tool developers, test developers, manufacturers, and assemblers. CDX participation comes from the main industry players and experts from a cross-section of industry across the above mentioned fields. Historically CDX participants included individuals and company representatives from Netronome, zGlue Inc, Ayar Labs, Broadcom, Macom, NXP, Microsemi, Broadpak, Socionext,



Marvell, Intel, ARM, Ansys, Boyd Corp, Mentor/Siemens EDA, Synopsys, Cadence, ASE, Applied Materials, Thrace Systems, Palo Alto Electron and others.

More information on OCP and ODSA can be obtained at the following URL link.

<https://www.opencompute.org/wiki/Server/ODSA>



Chiplet Modeling

Need for Chiplet Models

As general purpose chiplet providers offer their devices to market for use in heterogeneous package designs, it will be necessary that a standardized set of design models are provided to ensure operability in the EDA design workflows. In this paper, we propose models that include Thermal, Physical/Mechanical, Behavioral, Power, Power/Signal Integrity, Electrical, Test, Security as well as Documentation to facilitate the integration of the chiplets into a design. It is strongly recommended that these models are electronically readable for use in the design workflows. The models will leverage existing industry standards that are available and extensions and/or new standards will be defined as necessary. Table 3.1 below summarizes the proposed chiplet models to enable a usable chiplet ecosystem. Not all chiplets will require all of these models, but there must be a core set of deliverables provided to support the design integration, verification and testing of the chiplet IP into a System in Package (SiP) design. The scope of these models is currently targeted for 2.5D, interposer-based designs. Note that these 2.5D structures may include silicon interposers, silicon bridges or organic based fan-out technologies which can be considered as an “organic interposer”. Additional or modified deliverables will be required to address the needs of 3D designs.

Table: Models

Model	Description
Thermal	ECXML – JEDEC JEP181
Physical, Mechanical & IO	Library Exchange Format (LEF) GDSII or OASIS SPICE JEDEC JEP30-P101 Optional: Verilog to Physical Pin Mapping file (CSV)

Behavioral	<p>SystemVerilog (SV) IEEE – 1800-2017</p> <p>Recommended: Verilog-AMS 2.4</p> <p>Optional: SystemC IEEE – 1666-2011</p> <p>Optional: Bus Functional Model (BFM)</p>
Power	<p>Liberty (.LIB)</p> <p>IEEE2416 Standard for Power Modeling to Enable System Level Analysis</p> <p>Optional: Unified Power Format (UPF) – IEEE 1801-2018 or Chip Power Format (CPF)</p> <p>Optional: Verilog-AMS 2.4</p> <p>Optional: SystemC IEEE – 1666-2011</p>
Signal Integrity Analysis	<p>IBIS/IBIS-AMI</p> <p>Optional: Spice netlist (for the IO driver and/or receiver)</p> <p>Optional: Channel model</p>
Power Integrity Analysis	<p>Chip Power Model (CPM)</p>
Electrical Rules	<p>JEDEC JEP30-E101</p>

Test	Boundary Scan Description Language (BSDL) – IEEE 1149.1 BSDL – IEEE 1149.6/1149.7 ATPG model - Primitive/UDP based Verilog Internal JTAG (IJTAG) IEEE 1687 Optional: IEEE-1500 Core Test Language (CTL) description IP Firmware (required if applicable) Recommended: Gray-box level netlist Full-chip ATPG vectors - STIL (IEEE1450.1) or parallel wgl Full-chip Memory BIST/repair vectors - STIL (IEEE1450.1) or parallel wgl Optional : Unified Power Format (UPF) – IEEE 1801 or Chip Power Format (CPM)
Security	Optional: Security Agent
Documentation and Guidelines	General Chiplet Documentation SiP Physical Integration guidelines SiP Test guidelines Optional: Firmware (if applicable) Optional: Security

Chiplet Models

Thermal

Thermal models are required for each chiplet in a SiP design to perform package level thermal analysis. The information required by a thermal simulation tool for each chiplet component is provided in an industry

standard, ECXML – JEP30-T181 JEDEC model. This model includes a 3D description of the chiplet, material thermal properties and power maps summarizing the power profile of the device. A proposal to add support for arrays and spherical pins to the JEP30-T181 JEDEC model has been submitted by the CDX working group. The current standard supports a steady state power/thermal model, but a time based, piecewise linear (PWL) power profile may be considered in future updates to the standard to support transient thermal behavior of the SiP device.

The power map should provide adequate granularity of the chiplet component for use in the SiP level thermal analysis. This may include power estimates for each top level block and/or a 2 dimensional grid of power estimates for each grid element. The minimum requirement is a single block power estimate for the entire chiplet. The standard also supports a two-resistor thermal model, but this mode is not recommended for SiP level analysis.

Separate models should be provided for different functional modes of operation if applicable. A separate model for the major functional test modes should be provided if significantly different from the functional mode.

Physical, Mechanical & IO

Library Exchange Format (LEF)

The LEF chiplet model defines the two dimensional physical dimensions, layer and electrical net names of each chiplet bump pin. This model is used for SiP level physical design.

LEF models have been historically provided to define abstract layout views of ASIC IP macros used by ASIC Place and Route (PNR) tools. LEF views may also be used to define abstract layout views of internal ASIC macros and SiP level components including chiplets used by package planning, design and verification tools. The LEF views also include net signal information of the defined structures.

PNR LEF views often just include the X/Y coordinates of the center of the pin connection point. PNR LEF views may also include additional information not required for package design such as PNR blockages.

The design intent of LEF models used for package design differs from that of ASIC design and will generally require a different LEF model which we can refer to as a “Package” LEF model. A package LEF model should include all of the physical pin geometrical information required for the package design/verification process.

A chiplet Package LEF model should include the outline geometries of the chiplet die including the scribe line and the outer level geometrical boundary of the top level metal layer. It should also include the top level, 2

dimensional pin geometrical description of each pin, including micro-bumps, TSVs and probe pads along with the pin net name.

Note that it is common practice to perform a radial shrink to the organic substrate in packages including a silicon interposer to compensate for the different thermal expansion coefficients of the organic and silicon materials. The required shrink factor can be determined through thermal-mechanical stress simulations or based on manufactured test vehicles. The native, unshrunk version of the database may be useful for physical pin alignment checks between the silicon interposer and the package substrate. For manufacturing and final DRC/DFM checks, the shrunk database is required. A LEF model for the unshrunk database is sufficient, but it is recommended to provide GDS2/OASIS for both the shrunk and unshrunk versions of the package substrate if applicable.

Graphical Design System (GDSII) / Open Artwork System Interchange Standard - OASIS

The GDSII/OASIS chiplet model defines the two dimensional physical dimensions and layers of each chiplet pin. This model is used for SiP level DRC and LVS and for physical assembly. The GDSII format was established in the 1970's and remains a valid standard to this day. The OASIS format was established in the early 2000s' and includes constructs to more efficiently represent the geometrical information of large databases than the GDSII format. Both formats are generally supported by most ASIC and Package design tools and the formats can be readily translated back and forth from each other. Either format or both can be provided for chiplet models. A chiplet GDSII/OASIS model should include the outline geometries of the chiplet die including the scribe line and the outer level geometrical boundary of the top level metal layers. It should also include the top level, 2 dimensional pin geometrical description of each pin, including micro-bumps, through silicon vias (TSV)s and may optionally include probe pads. If the assembler requires alignment keys for assembly purposes, these structures should also be included in the chiplet GDSII/OASIS model. Pin net names may also be optionally defined by attaching text properties to the respective pins.

SPICE

The electrical connectivity of a SiP-level design is verified using a LVS design flow. Since the chiplet components of the design are fixed, only the connections to the top-level chiplet pins need to be defined and verified for the SiP design. To support this flow, a SPICE level netlist model is provided for each chiplet, defining the top-level cell name and all of the top-level external pins, including micro-bumps, TSVs, and optional probe pads. It is

recommended that these pin names be consistent with the LEF, GDS, and functional SystemVerilog (SV) pin names.

JEDEC JEP30-P101

JEDEC JEP30-P101 is the model used to define the mechanical and IO properties, tolerances and pertinent information for all chiplet and associated, external pins for use in SiP level connectivity and assembly.

There are several different types of physical pin interconnect technologies used to connect the chiplet die to the interposer/bridge and/or substrate. For 2.5 applications, these pin types generally include micro-bump structures used to connect the die to the interposer or silicon bridge and TSVs used to connect the die, through the interposer to the substrate. The micro-bump structures are process specific and may include copper pillar or solder ball interconnect. The TSV structures are also process specific. Additionally, probe pad structures are generally included on the chiplet die to support wafer level testing of the die prior to package assembly.

This model requires a three dimensional description as well as the material properties of the connectivity structures. This information is required for the design and verification of the SiP and by the chip assembler. The delivery mechanism of the actual chiplet devices should also be defined as either a wafer level or singulated die. This information is used in the SiP assembly process.

The zGlue Exchange Format (ZEF) is an open source format used to define mechanical, IO and electrical information for packaged devices. The ZEF format is in the process of being migrated to an XML format and will be referred to as “ZEFXML”. A variant of this format is being considered to define relevant mechanical, IO and electrical information for unpackaged, chiplet devices.

The mechanical and IO sections of the new ZEFXML open standard will be proposed as a new format for packaged and unpackaged chiplets. The mechanical information would be JEP30-P101 and IO JEP30-E101 schemas.

Optional: Verilog to Physical Pin Mapping file (CSV)

It is recommended that all pin names are consistent with the LEF, GDS and functional SV pin names where possible.

If the Chiplet functional pin names defined in the chiplet SystemVerilog (SV) models are not identical to the pins defined in the LEF and/or GDS mapping file, a CSV table is provided to map the associated functional pins in the SV model to the SPICE, LEF and/or GDS pins.

Behavioral

Behavioral models for each chiplet component are required to support the SiP level and optional system level functional simulations. Verilog is an IEEE standard hardware description language used to model the functionality of an electronic system. These models are used by functional simulators to simulate the component, SiP and system level behavior of the electronic system. For chiplets that contain analog functionality, the analog extension of Verilog, Verilog-AMS should be considered. SystemC is another optional format that chiplet vendors may support for use in higher level, system level analysis and optimization.

SystemVerilog (SV) IEEE – 1800-2017

SystemVerilog is a superset of the Verilog HDL language and includes provisions to develop functional verification test benches. Chiplet vendors should provide accurate functional models for their device for use in SiP level and system level functional simulations.

Chiplet vendors may optionally consider providing test benches written in SV for use in unit level testing of the device in the context of the SiP and/or system level functional verification.

Recommended: Verilog-AMS 2.4

Verilog-AMS is an extension of the Verilog hardware description language (HDL) and includes constructs to model analog functionality and structural descriptions of mixed signal circuits and systems. It is now the standard language for device modeling (replacing C in SPICE). Chiplet vendors may optionally consider providing Verilog-AMS models of their device in addition to the SV model(s). This is generally recommended for chiplet components that include analog functionality. The models can be used with RTL and/or circuit level simulation tools. Additional information such as analog behavior, thermal, cost may also be included at the discretion of the chiplet vendor.

These models can be used to model the chiplet in the context of a SiP and/or system level simulation. It can also be used for architectural exploration and performance modeling. The primary advantage of Verilog-AMS over

other languages in the context of chiplets is that it uses “disciplines” to mark wire types, which includes electrical, thermal, fluid, optical and possibly RF at the level of stitching chips or chiplets into systems. While mixing disciplines on “wires” is illegal in Verilog-AMS, other HDLs just consider everything as electrical, and it’s easier to make mistakes. Discipline information can easily be stripped out for Verilog compatibility.

Optional: SystemC IEEE – 1666-2011

Optional Functional model for the chipllet written in SystemC to be used for electronic system level or transaction-level modeling of the chipllet in the context of a SiP and/or system level simulation. It can also be used for architectural exploration, performance modeling and software development. Chipllet vendors may optionally consider providing SystemC models of their device in addition to the SV model(s). The models can be used with system level design/analysis tools. Additional information such as analog behavior, thermal, cost may also be included at the discretion of the chipllet vendor. These models can be used to model the chipllet in the context of a SiP and/or system level simulation. It can also be used for architectural exploration, performance modeling and software development.

Optional: Bus Functional Model (BFM)

Some chipllet devices, such as processing devices, may include cycle accurate, bus functional models (BFM), which may be used for SiP and/or system-level functional verification. If the model is in the Verilog format, it can be used in addition or in lieu of an SV model.

Power Dissipation

Liberty (.LIB)

Liberty models include power models for the chipllet based on clock period and core/IO operating voltage levels. This model may be used to model the power of the chipllet in the context of a SiP and/or system-level simulation. Separate models should be provided for different functional modes of operation, if applicable. A separate model for the major functional test modes should be provided if significantly different from the functional mode.

IEEE 2416

The IEEE 2416 power modeling standard analyzes chiplets based on equation, measured, or simulated data. A single model can capture power at different operating modes. Power should be provided for test modes if significantly different from the functional modes.

Unified Power Format (UPF) – IEEE 1801-2018 or Chip Power Format (CPF)

The Unified Power Format (UPF) or Chip Power Format (CPF) models are used to define the power intent and power implementation of the chiplet device, including all unique power domains and supplies. The chiplet UPF/CPF models can be used by the SiP package and/or system design teams to plan, implement, and verify the power delivery to each chiplet within the SiP package design. Separate models should be provided for different functional modes of operation, if applicable. A separate model for the major functional test modes should be provided if significantly different from the functional mode.

Signal Integrity Analysis

IBIS/IBIS-AMI

Input/output buffer information specification (IBIS) models are a simplified model of I/O buffers run on a spice-like simulator for board and SiP level Signal Integrity analysis. The traditional IBIS model is an ASCII, table based current vs voltage (I-V) model and includes parasitic RC information of the buffers.

IBIS-AMI models are a more complex model of I/O buffers run on a Serdes channel simulator for high speed, board level Signal Integrity analysis. These models include two ASCII files (.ibs and .ami) and a platform specific executable model (.dll window, .so Linux). These models are generally required for multi-gigabit serial links.

The IBIS models are a simplified model which allows an IP provider to hide the details of I/O buffer design. Alternatively, the chiplet vendor may provide a detailed or simplified spice netlist of the I/O buffers in addition to or in lieu of an IBIS model.

Chiplet vendors may provide optional channel models for the high speed, D2D interfaces to assist signal integrity engineers in the setup and analysis of these interfaces. The channel requirements on these D2D interfaces should be defined in a tool readable format by the respective chiplet and SOC-PHY vendors. Touchstone models are used to define insertion loss, return loss and crosstalk specification. Eye diagram specifications (eye mask width and height) can be captured in an XML format. We will consider recommending adding an eye diagram specification to the JEP30-E101 JEDEC standard.

Power Integrity Analysis

Chip Power Model (CPM)

CPM is a de facto standard used to model the static and transient power profile of a full die including the internal resistor-inductor-capacitor (RLC) parasitics of the chiplet power delivery network through the power and ground pins of the chiplet. The models are used to perform spice level power integrity analysis at the board and SiP level. Separate CPM models should be provided for different functional modes of operation if applicable. A separate model for the major functional test modes should be provided if significantly different from the functional mode.

Electrical Properties

JEP30-E100 is a JEDEC standard that includes electrical and functional properties for parts and associated terminals. We propose using this standard to capture the electrical and functional properties for a chiplet part and its associated pins (i.e., terminals).

The property values can be specified with or without conditions. The JEP30 schema is a container where properties can be specified with values, conditions and equations. Additional properties unique to chiplet devices may be added and/or removed to the existing standard. Chiplet vendors can adhere to the standard values and/or specify their own values.

ZEF (zGlue Exchange Format) is an open source format used to define mechanical, IO and electrical information for packaged devices. ZEF is defined in CSV format. ZEFXML is an enhancement of ZEF in XML format for better support in multiple values data, grouping of data, custom unit and data. It is schema based and described in XML Schema Definition (XSD) and easily extensible with backward compatibility to older versions.

There are three data exchange XML files as defined below. Each of them defined by the associated XSD file.

- Mechanical - All x,y,z, tolerance, solder type and material properties
- IO - Pin location, functionality, mode of operation, electrical characteristics (EC), abs max values, operating conditions, allowable RLC, voltage references, temperate based voltage and current (VI) pin characteristics
- Electrical - Contains overall absolute maximum ratings, recommended operating conditions, ESD ratings and electrical characteristic such as root mean square (RMS) current limit

There is a XSD file defining the schema associated with each file type. The first line of each file consists of the file description followed by the name and value pair for each parameter.

- mech_zef.xsd
- io_zef.xsd
- elect_zef.xsd

The filenames follow a convention naming of <OPN>_<TYPE>_zef.xml where:

- OPN - Orderable Part Number which is a unique product identifier from the manufacturer
- TYPE - Represents the type of file either MECH, IO, or ELECT

For example, a BQ27426YZFT Chiplet would have:

- BQ27426YZFT_mech_zef.xml
- BQ27426YZFT_io_zef.xml
- BQ27426YZFT_elect_zef.xml

ZEF and ZEFXML information is available on github at <https://github.com/zglue/zef>.

Sample properties for chiplet safe operating areas (SOA) and conditions are summarized as follows:

- Voltage levels on pins
- Max RMS current limit on pins and bumps, when applicable
- Max capacitance (also defined in .LIB)
- Allowed Voltage overdrive/underdrive
- ESD rating
 - Human Body Model (HBM)
 - Charge Device Model (CDM)
 - Machine Model (MM)
- Thermal limits
 - Min/max junction
 - Allow for equation
- Future considerations:
 - Shock and vibration rating
 - RadHard rating
 - Power sequencing
 - Static voltage scaling map
 - Dynamic voltage scaling
 - RFI emission tolerance

Test

Integrating multiple ASIC (chiplet) devices into a single package presents several challenges in testing the individual chiplet devices as well as the device-to-device (D2D) interfaces between the chiplets. Although chiplets are delivered by respective chiplet vendors as pre-tested, known-good-die (KGD) [1] devices, during the assembly process it is possible that a chiplet device and/or the D2D interconnect is damaged or defective. As such, there is still a requirement to test the individual chiplets. To facilitate this in-package testing, the chiplet vendors will need to provide the respective manufacturing test patterns to ensure the device is still operational after it is assembled into the SiP package. It is also necessary to test each of the D2D interfaces between all chiplets with slow and at-speed interconnect testing. Since many of the test pins of the individual chiplets may not be available through external package pins, advanced 2.5D and 3D test access [4] and methods [9] are required.

Production testing of traditional ASIC devices utilize structured DFT tests as the primary test methods. Boundary Scan [2] is used for IO and interconnect testing, MBIST/repair for internal memory testing and scan testing for internal digital logic. Analog or IP testing utilizes additional testing techniques including functional patterns, loopback and other Built-In Self-Test (BIST) logic tests. The individual chiplet tests, D2D tests and any top level IP tests are combined to a complete ATE production test program for the multi-die, SiP device. The SiP integrator may also include additional, SiP level functional tests.

The BIST and IP-related ATE tests are accessed or initialized through a standard IEEE-1149.1 [2] TAP serial interface which typically runs at a slow clock rate of 10 to 50 Mhz. JTAG [3] is the preferred method of internal test access for DFT/BIST and IP testing. Chiplet scan testing will need to accommodate IO overrides at the package pins, as well as coordinated feedthroughs through the chiplets to support standard scan techniques and newer methods such as packet based scan [6]. In SiP designs with multiple chiplets, the TAP TDI/TDO test pins are serially connected from chiplet to chiplet, connected through the interposer. Since these serial pins are serially “daisy chained” in the SiP, the operational speed of the JTAG IO will be limited by the slowest chiplet BSCAN speed. Additionally, SiP designs with large interposers and many chiplets will have interposer routing parasitic delays which could further reduce the operational test speed of the SiP device. To minimize these delays, careful interposer test routing and SiP planning are required as well as static timing analysis and/or timing simulation to verify the SiP interconnect delays.

IP test methods may incorporate serial or parallel D2D functional interfaces. Techniques such as in-package SiP boundary scan and IO BIST with lane redundancy and repair [5] may be used during production test and functional operation to boost overall SiP yield. Serial D2D interconnect test techniques may include near-end/far-end and D2D Serdes loopback. These test techniques are typically provided with the IP core. Chiplet vendors need to provide full documentation for IP test and integration, as well as supporting PDL/ICL files to simplify SiP level pattern generation and simulation.

The power of the chiplet devices operating in their respective test modes may be significantly higher than the functional mode power. Careful power planning, analysis, and control are required [7].

An additional challenge in testing SiP devices with multiple chiplets is debugging failing test patterns of an embedded chiplet. In traditional ASIC devices, IP vendors will provide test/diagnostic support as required to the ASIC test team for their respective IP. A chiplet vendor will provide test patterns and guidelines to assist the SiP test team in developing a SiP level test program. A chiplet may be very difficult to debug should it fail SiP level testing. The ownership and responsibility for chiplet debug and failure analysis is an issue that will need to be addressed between the chiplet vendors and SiP test teams. The chiplet vendor should provide enough models, netlists, and design information for the SiP assembler to easily debug D2D test failures and interconnect tests. Several of the published test standards and chiplet deliverables are summarized in the following.

Boundary Scan Description Language (BSDL) – IEEE 1149.1 [2], IEEE-1149.6

Chiplet boundary scan model used for slow speed IO and interconnect testing within the package and external to the package at the system and board level. Supports DC and AC coupled interfaces as required.

ATPG model - Primitive/UDP based Verilog

Generic Standard Cell and IO model used to test logic and interconnect are required, EDA-vendor specific models for all major EDA vendors are optional.

Internal JTAG (IJTAG) IEEE 1687

Test patterns for chiplet IP and MBIST/repair tests

Instrument Connectivity Language (ICL)

Used to describe the internal test structures of the device under test

Procedural Description Language (PDL)

Used to create test patterns for IP like SerDes and specialized tests

Used to create chiplet test initialization sequences like PLL initialization for die-to-die (D2D) at-speed scan test

Optional: IEEE-1500 Core Test Language (CTL) description

Required for 2.5D chiplets that have HBM PHYs

IP Firmware (required if applicable)

For Test initialization of chiplet and/or IP PHYs that are embedded in a chiplet.

Recommended: Gray-box level netlist

Gray-box level netlist of test logic interfaces to support functional and timing simulation of chiplet production test patterns.

- Scan
- Boundary scan
- 3D: All IEEE1838 logic including PTAP/STAP, DWR, 3DCR, etc

Min/Typ/Max SDF: timing files for all supplied netlists.**Full-chip ATPG vectors - STIL (IEEE1450.1) or parallel wgl**

Automatic Test Pattern Generation (ATPG) vectors generated by DFT test tools to test the internal logic of the chiplet device through the chiplet IO pins.

Full-chip MBIST/repair vectors - STIL (IEEE1450.1) or parallel wgl

MBIST vectors generated by DFT test tools to test the internal memories of the chiplet device through the chiplet IO pins.

Optional : Unified Power Format (UPF) – IEEE 1801 or Chip Power Format

UPF/CPF models for the chiplet, defining the power intent and implementation of the chiplet device including all unique power domains and supplies.

Optional: Security Agent

Hardware and/or software provided with the chiplet to enable the end user of the SIP to assure the Trusted Supply Chain Traceability of the respective chiplet. The security agent is optional, but may be required for certain security-critical use cases.

The chiplet die is authenticated with a system-level root-of-trust device (for example: [OpenTitan](#)), using established cryptographic authentication techniques. An example of such a technique is: ‘Physically Unclonable Functions (PUF)’[13]. Once successfully authenticated, the chiplet will become accessible by the SIP, and data transfers to the SIP will be enabled. No data transfers to the chiplet should be allowed if the authentication method fails. The chiplet will silently ignore all data accesses by the SIP until the authentication is successful. Unsuccessful authentication attempts are to be reported to the SIP, and the reason for the authentication failure is to be recorded by the SIP.

Hardware and/or software provided with the chiplet to enable the end user of the SIP to assure the Trusted Supply Chain Traceability of the respective chiplet.

The security agent provides cryptographic authentication of the chiplet to a system level root-of-trust. Software images downloaded onto the chiplet die, or used to update embedded firmware on the chiplet die must be cryptographically signed. The authenticity of this signature must be verified by the system-level root-of-trust prior to using the software update, or executing the software update on the chiplet die.

An example of a possible security agent is ‘Physically Unclonable Functions (PUF).’

Documentation and Guidelines

Although it is strongly recommended to provide all chiplet models and specifications in a machine readable format, it is still necessary to provide documentation to describe the functionality and operation of the chiplet as well as guidelines to facilitate the integration, functional/physical verification, analysis and ATE production testing of the chiplet into a SiP design.

General Chiplet Documentation

An IC datasheet is provided for all ASIC components and generally includes a detailed description of the device, pinout, operating conditions and electrical/mechanical specifications. A datasheet should be provided for a chiplet including similar information that would be provided in an ASIC data sheet. Since a chiplet is unpackaged, specific package information would not be applicable. However, information should be provided to describe the packaging technology that the chiplet can deploy for integration into a SiP design. Where applicable, the chiplet vendor should document the package assembly vendor/process that the chiplet is compatible with. Detailed models are also provided for the design and assembly of chiplet into a SiP device as outlined in the other modeling items included in this section.

SiP Physical Integration guidelines

SOC IP vendors generally provide integration guidelines that are used by IC and package design teams to integrate their IP into a custom ASIC design. These guidelines include information on how to simulate, integrate the IP into an ASIC block or floorplan and verify the physical and electrical integrity of the IP. They also include checklists, package guidelines/requirements and any other general information that would assist the design team to successfully integrate the IP. Some vendors will provide optional consulting support and/or support a design review with the design teams to ensure the IP is integrated and verified in compliance with the guidelines. A similar set of guidelines for chiplet IP should be provided by the respective vendors to be used by IC and package design teams to integrate their IP into a custom SiP design. Optional consulting support and/or design review support should also be considered.

SiP Test guidelines

SOC IP vendors generally provide test guidelines that are used by the DFT and Test teams to support the DFT insertion and ATE test program development of their associate IP. Additional guidelines may also be provided to support the end customer in bench testing and bring-up of the device. Similar test guidelines for chiplet IP

should be provided by the respective vendors to be used by the DFT, ATE and functional bring-up Test teams to support the ATE and functional testing of the respective chiplet within the context of the SiP design.

Optional: Firmware (if applicable)

Some chiplets may include internal IP or logic that requires firmware to test and/or configure the IP for use in the end application. Where applicable, chiplet vendors should provide the firmware, detailed guidelines, documentation and scripts as required to support the test and/or configuration of the respective chiplet within the context of the SiP design.

Optional: Security Guidelines

Documentation, guidelines for hardware and/or software integration of security to support the end user of the SiP to implement and/or operate security agents assuring the Trusted Supply Chain Traceability of the respective chiplet.

Power Estimation of Multi Die Systems: Models and Workflow

Accurate power dissipation and energy consumption estimates are a crucial part of the multi die system design process. Overall, power and energy estimation serves to ensure multiple design limits are met, including:

- Thermal limits - ensuring that the system stays below a maximum temperature
- Energy limits - any battery power application will have a battery lifetime target
- Maximum current draw - power supplies need to be sized to allow for maximum currents to be delivered
- Maximum current step load - power supplies need to be designed to support a given load current step while maintaining voltage levels

Complicating the effort of power estimation is that the above limits do not occur under the same assumptions and conditions. For example, thermal dissipation is affected by both amount of power dissipation and by time period for which it needs to be dissipated and requires an engineer to understand both power dissipation and operation over time, as a result, the worst thermal case may not coincide with the worst power case. Similarly, energy estimation requires understanding of operation over long periods of time and because of this it is possible that the energy limits are dominated by the lowest power dissipation operation. In the same category, worst current load ramp will probably not occur at the same time as worst power or worst thermal cases.

Confounding the problem of power estimation is the fact that different dies may be at a different stage of their design process. For a fully heterogeneous system, some dies may be completed and fully characterized, while others, as a result of disaggregation, may be just starting the design process.

Requirements for Power Modeling

Any power modelling approach needs allow for consideration of all system design limits - thermal, energy and currents.

It also needs to consider the accuracy requirements and available data.

It is typical when working on architecture exploration to use quick equation-based analysis.

The analysis can be refined as the chiplets progress through the design flow. And finally, actual silicon measured and characterized data can be used to validate assumptions.

A System-level Power Model must meet several criterias:

- It must enable architectural exploration, where a user can derive estimates under different conditions, including environmental, such as temperature and voltage, as well as usage, such as usage scenarios and settings.
- It must enable progressive updates and refinements of its internal data, where the provider of the data can represent the most recent data.
- It must be capable of handling data in different formats, so that it can represent datasheets, measurements, rough estimates, gate-level data, and even data with spice-level accuracy.
- It must be able to handle digital and mixed-signal models seamlessly

The data security aspect of chiplet power models should be carefully considered. As chiplet integration from multiple vendors becomes mainstream there will be a need for better accuracy of the power modeling. With power being deeply connected to the actual design, the model will then need to be a closer and more detailed representation of the die. This will raise data security issues - how do I share with my customer enough information so that they can perform the analysis they need, but without giving them the full design information?

Available Tools, Formats, and Solvers

Liberty

Liberty is a text based open file format. It is primarily used in the chiplet implementation and sign-off flows. It includes energy, leakage power, timing and delay information, as well as current waveforms.

For digital IPs this file is usually generated by characterization tools which would run circuit level simulations to obtain the data. A file with the subset of the data maybe generated form custom flow or signoff tools.

Major draw-back of Liberty when representing power for mixed signal and analog IPs is the need to model all power as based on pin transitions and as function of capacitive load and input ramptime.

IEEE2416 Standard for Power Modeling to Enable System Level Analysis

EEE2416 is a new power modeling format that enables generation of models at the system level, and meeting some of the requirements of a System Level Power model. Thrace System's PowerMeter tool expands beyond IEEE2416 by adding support for mixed signal IPs, various additional data types, and full hierarchical representation.

Some of the capabilities of a System-level Power Model were demonstrated on the OmniChip system. The results included maximum power, total energy and maximum current, all from within the same simulation.

Verilog-AMS

Verilog-AMS uses “[disciplines](#)” to indicate the domain of a wire - electrical, thermal, optical, etc. - cooling and RF connections are possible in a chiplet system, additionally you can tag ports/wire with direction and arbitrary attributes. The extra information makes it easier to correctly connect a thermal energy source into a heatsink model, or an optical driver with an optical receiver on another chiplet through an interposer waveguide.

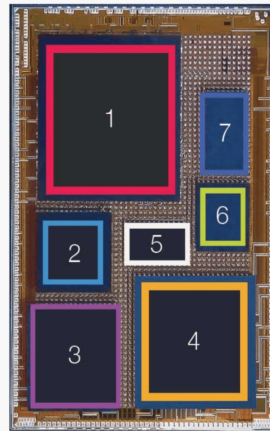
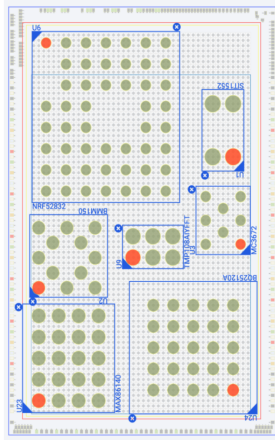
Verilog-AMS descriptions are interoperable with other flavors of Verilog, and unsupported features can be excluded with preprocessor directives (`#ifdef...`). Verilog-AMS is functionally a superset of SPICE, so most SPICE dialects are easy to translate into Verilog-AMS, but no SPICE dialect is an acknowledged standard.

Verilog-AMS is also a behavioral modeling language that can support fast models as well as detailed models, it is expected that detailed models for analog electrical and thermal behavior (PDE) will be replicated with automation tools into faster behavioral models (event-driven) for system level verification.

Power Modeling Workflow Examples

To demonstrate an application of a system level power model we worked with a design contributed to CDX by zGlue. The design is a 7 chiplet system designed for industrial and consumer IoT applications and includes MCU, BLE connectivity, temp sensor, accelerometer.

OmniChip Reference Design



- 1** Nordic nRF52832 MCU with BLE
- 2** Bosch BMM150 Magnetometer (direction detection)
- 3** Maxim MAX86140 Heart-rate monitor/optical pulse oximeter
- 4** Texas Instruments BQ25120A Battery charger
- 5** Texas Instruments TMP108 Temperature sensor
- 6** mCube MC3672 Accelerometer (motion detection)
- 7** SiTime SIT1552 32 kHz oscillator

Package options: Approx. 12mm x 12mm x 1.5mm QFN or 9.5mm x 6.8mm x 1.3mm LGA

zGlue

zGlue Confidential and Proprietary

1

Figure X: OmniChip reference design

Waveform		Configuration	
+POWER	AS TEXT		
Time	Power	Computed time	Computed power
0	$40 \cdot 10^{-3} \text{V}$	0ns	$120 \mu\text{W}$
$27 \cdot 10^6$	0	27000000ns	0W
$1/cr \cdot 10^9$	0	250000000ns	0W

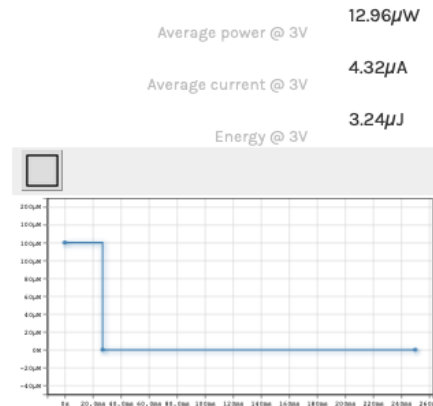
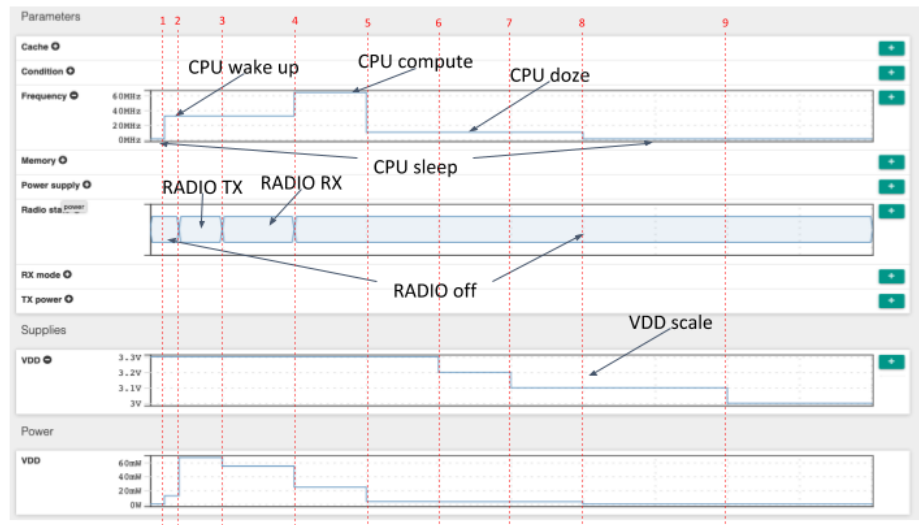


Figure X: Texas Instruments TMP108 power model showing duty cycle and power consumption dependency on input parameters V and cr

MCU Scenario definition and power analysis

1. CPU wake up for processing
2. Begin TX
3. TX done, begin RX
4. RX done, compute result
5. Doze
6. Lower voltage
7. Lower voltage again
8. CPU sleep
9. Lower voltage again



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Figure X: Example of OmniChip MCU scenario definition

Recommend Power Modeling WorkFlows

What's the start - chip, model, scenario, budget

Flow chart of who provides what and uses what

Thermal Design: Design Choices, Models, Workflow

Thermal Design Choices

Although impressive progress has been made on electronic cooling systems in recent years, the high heat flux removal from the high-tech electronic devices remains very challenging and inadequate. Based on heat transfer effectiveness, cooling modes can be classified into four general categories which are:

1. Radiation and free convection
2. Forced air cooling
3. Forced liquid cooling
4. Liquid evaporation or two phase liquid cooling

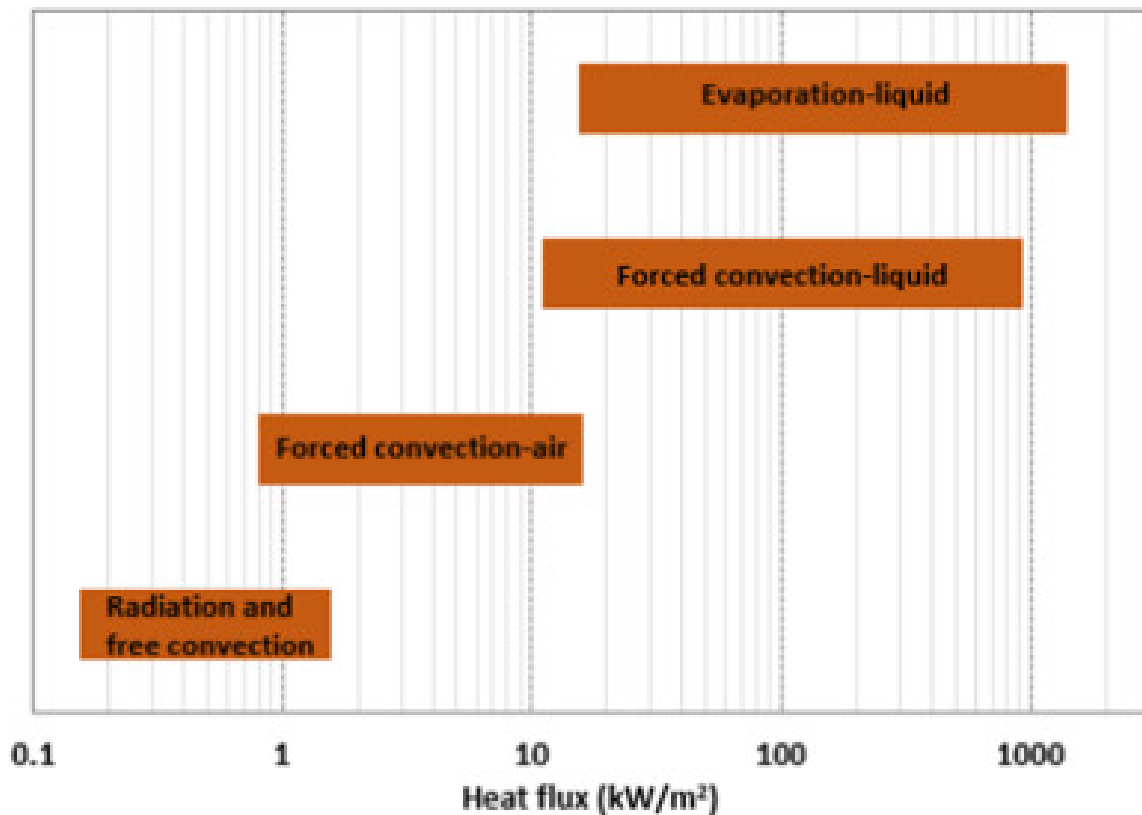


Figure 2: Comparisons of heat transfer effectiveness of conventional methods [ref: S.M. Sohel Murhsed, C.A. Nieto de Castro, Acritical review of traditional and emerging techniques and fluids for electronics cooling, Renewable and Sustainable Energy Reviews, Vo 78, Page 821-883]

Thermal management of multi-chip heterogeneously integrated systems poses additional constraints and limitations beyond those for single chip modules. When various chiplets are integrated into a package, it is

important to choose appropriate cooling solutions, which is mainly driven by the system level design, heat flux from the package, as well as the cost considerations. Below is a table summaries the typical cooling limitation among different cooling solutions, varying from air, single-phase liquid cooling or two-phase cooling:

Table X: Comparison of system cooling capabilities [ref: HIR1_ch20]

Thermal Solution	High end chip scale heat flux	Cost
Natural convection without heatsink solution	0-5 W/cm ²	0.\$
Traditional enhanced air cooling with heat pipe and/or extended fin	50 W/cm ²	\$
Advanced multi-chip air cooling with integrated vapor chamber on the lid	85 W/cm ²	\$\$
Water cooled module level passive cold plate	250-325 W/cm ²	\$\$\$
Water cooled chip scale cold plate	390 W/cm ²	\$\$\$
Micro channels in the device with single phase water flow	790 W/cm ²	\$\$\$\$

There are lots of assumptions embedded in the table above, factors such as TIM material selection, ASIC package design, junction temperature limitation, system form factor, will all impact the final possible cooled heat flux value. The table above provides the highest possible range according to either commercially available or demonstrated system solutions.

Requirements for Thermal Model

Thermal model of a chiplet requires combining information of 4 different types of data

- 3D description of the of the chiplet
 - This description needs to include all geometry components of the chiplet, including dies
- Material properties
 - Material properties are required for solving the basic heat flow equations. Material properties need to include thermal conductivity for steady state analysis and specific heat and density for transient simulations
- Heat sources

- Heat source description needs to include location, dimension and either a total power (W) or power density (W/m²)
- 3D description of the external system, if applicable
 - Fans, world dimensions, etc.

It is highly recommended that chiplet vendors characterize and correlate thermal models.

A system designer will use this information and combine with models for other components and run their thermal simulation.

ECXML - JEDEC JEP181

ECXML is a standard developed and released by JEDEC as JEP181. It was officially released in September 2020 and full description can be found on the JEDEC website. Below is a brief description of ECXML

ECXML uses XML to describe 3D systems and includes constructs to allow description of the necessary 4 required components listed in 5.1. 3D objects can be described as boxes with defined dimensions and location, as well as material they are made of. Materials can be provided and be defined as isotropic or anisotropic and can be referenced by 3D objects. Heat sources can be described as either 2D or 3D objects with a total power dissipated. And lastly, it allows for the description of the whole system.

Since ECXML includes all necessary data it is the recommended data delivery format for thermal simulations.

ECXML has a few drawbacks. It lacks the ability to describe spheres, which may be used to describe bumps and pillars. This is considered to have negligible effect on accuracy of final thermal results. It also describes power as a static number and lacks the ability to specify time based power. This can be easily worked around by providing one file per “power mode”.

There are other formats that describe some of the 4 parts, but not all 4. For example, STEP can describe any 3D geometry, however, it does not include materials or heat sources. Using STEP requires custom scripts to post-process the geometries and to combine with material and heat data. It is recommended that the chiplet vendor perform this and still deliver ECXML with their chiplet.

Thermal Modeling Workflow Examples

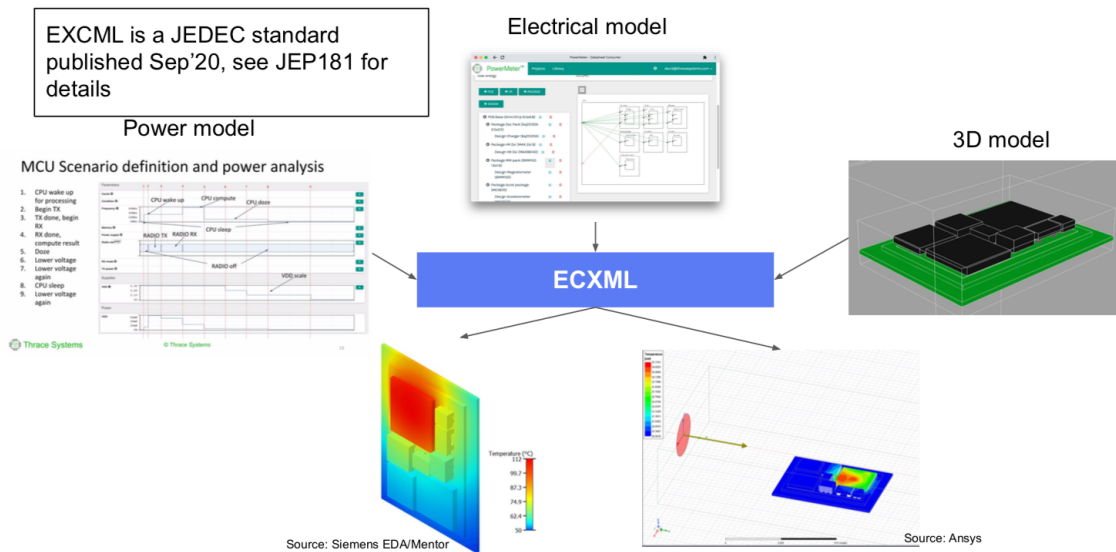
To demonstrate the use of ECXML we created a file and used it to run thermal simulations. To create the file we used data from the following sources:

- 3D geometries came from STEP file
- Material properties were assigned based on publicly available data
- Power came from the simulation done in Chapter 4

A custom script was developed for FreeCAD to write out the data.

The resulting ECXML was provided for simulation into industry standard tools. Below is a flow chart of the process.

ECXML for thermal analysis



Source: David Ratchkov, ODSA, xxxxx 2021.

Recommend Thermal Modeling WorkFlow

Recommendation is chiplet vendors to deliver EXCML for their chiplets to enable integration of the chiplet ECXML into the larger system simulations.

Recommend provide ECXML for major modes, to allow Function and Test Thermal analysis, and Mechanical simulations for functional operations.

Conclusion

Chiplet are becoming increasingly common in today's packaged systems design. In this paper, we have proposed models that include Thermal, Physical/Mechanical, Behavioral, Power, Power/Signal Integrity, Electrical, Test, Security as well as Documentation to facilitate the integration of the chiplets into a design. Two examples were provided of using the recommended model for Power Estimation and Thermal Analysis.

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